Semester - 4
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Unit 4

Interrupts

Interrupt

In digital computers, an interrupt is an input signal to the processor indicating an event that needs immediate attention.

An interrup signal alerts the processor and serves as a request for the processor to interrupt the currently executing code, so that the event can be processed in a timely manner.

Interrupts in 8085 microprocessor →

When microprocessor receives any interrupt signal from peripheral(s) which are requesting its services, it stops its current execution and program control is transferred to a sub-routine by generating CALL signal and after executing sub-routine by generating RET signal again program control is transferred to main program from where it had stopped.

When microprocessor receives interrupt signals, it sends an acknowledgement (INTA) to the peripheral which is requesting for its service.

Interrupts can be classified into various categories based on different categories →

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1. Hardware and Software Interrupts
When microprocessor receive interrupt signals through pins (Hardware) of microprocessor, they are known as Hardware Interrupts in 8085 MP.
They are —
INTR, RST 7.5, RST 6.5, RST 5.5
TRAP.
Software Interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor.
These are 8 software interrupts in 8085 microprocessor.
They are —
RST_0, RST_1, RST_2, RST_3, RST_4, RST_5
RST_6, RST_7.

2. Maskable and Non-Maskable Interrupts
Maskable interrupts are those which can be disabled or ignored by the microprocessor.
These interrupts are —
edge triggered or level triggered.
So they can be disabled.
INTR, RST 7.5, RST 6.5, RST 5.5 are maskable interrupts in 8085 microprocessor.
Non-Maskable interrupts are those which can not be disabled or ignored by the microprocessor.
TRAP is a non-maskable interrupt.

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It consists of both level as well as edge triggering and is used in critical power failure conditions.

3. Vectored and Non-Vectored Interrupts

Vectored interrupts are those which have fixed vector address and after executing these, program control is transferred to that address. (RST0 — RST7)

Non-Vectored interrupts are those in which vector address is not predefined. The interrupting device gives the address of subroutine for these interrupts.

INTR is the only non-vectored interrupt in 8085 microprocessor.

Priority of Interrupts

When microprocessor receives multiple interrupts requests simultaneously, it will execute the interrupt service request (ISR) according to the priority of interrupts

TRAP — Highest
RST 7.5
RST 6.5
RST 5.5
INTR — Lowest

Instructions for Interrupts

1. **Enable Interrupt (EI)** → The interrupt enable flip-flop is set and all interrupts are enabled following the execution of next instruction followed by EI.
   After a system reset, the interrupt enable flip-flop is reset, thus disabling the interrupts.
   This instruction is necessary to enable the interrupts again (except TRAP).

2. **Disable Interrupt (DI)** → This instruction is used to reset the value of enable flip-flop hence disabling all the interrupts. No flags are affected by this instruction.

3. **Set Interrupt Mask (SIM)** → It is used to implement the hardware interrupts (RST 7.5, RST 6.5, RST 5.5) by setting various bits to form masks or generate output data via the Serial Output Data (SOD) line.

4. **Read Interrupt Mask (RIM)** → This instruction is used to read the status of the hardware interrupts by loading into the A register by a byte which defines the condition of the mask bits for the interrupts. It also reads the condition at SID (Serial input data) bit on the microprocessor.

Edge triggering is a type of triggering that allows a circuit to become active at the positive edge or the negative edge of the clock signal.

Level triggering is a type of triggering that allows a circuit to become active when the clock pulse is on a particular level.

Restart interrupts → These interrupts occurs when the operator selects the restart function at the console or when a restart signal processor instruction is received from another processor.

Questions →

1. Which interrupt has highest priority?
2. List the four instructions which control the interrupt structure of 8085 HP.
3. What is meant by interrupt?
4. Explain the priority interrupts of 8085.
5. How many interrupts does 8085 have mention them.